

## DFT Manager

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Company: NodeFlair

Location: Ho Chi Minh City

Category: computer-and-mathematical

### Main Responsibilities:

Collaborate with cross-functional teams to define and develop design for testability (DFT) strategies for automotive silicon chips, including ADAS SoC, Mega MCU, and Gateway SoC.

Design and implement RTL code, incorporating DFT structures, using DFT insertion tools or using hardware description languages (HDL) such as Verilog or System Verilog.

Develop and execute test plans and verification strategies to ensure designs meet DFT goals in automotive industry standards.

Design and develop in-system test environments, including hardware and software components, to enable efficient testing and validation of RTL designs in the context of the target automotive system.

Debug and resolve design and verification issues related to DFT and especially in in-system test environments, working closely with other design and verification engineers to ensure robustness and efficiency of RTL designs.

Keep up to date with industry trends, best practices, and new technologies in automotive silicon chip design, with a focus on DFT and in-system test environments, and proactively contribute to continuous improvement initiatives.

### Requirements:

7~10 years of RTL design experience with Verilog or System Verilog

English required for reading technical documents such as international standards or user manuals for tool set-up.

Familiar to IEEE1149/1500/1687 standards

Experience with Tessentshell / Testkompres for ATPG

Experience with Tessent MBIST and In-System Test

Preferred: Knowledge of scripting languages PERL or TCL or knowledge of C/C++ is a plus

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